INTEL CORP. v. PACT XPP SCHWIEZ AG, Appeal No. 2022-1037 (Fed. Cir. March 13, 2023). Before Newman, Prost, and Hughes. Appealed from the Patent Trial and Appeal Board.

Background:

Intel petitioned for *inter partes* review of claims 4 and 5 of PACT's patent directed to multiprocessor systems and how processors in those systems access data. At issue was independent claim 4 which recites an interconnect system that monitors and maintains cache coherency by identifying inconsistencies of local copies of data among different caches. Specifically, the parties disagreed on whether the prior art could be combined to render obvious the "segment-to-segment limitation" of claim 4 directed to a separated cache formed by segments.

During the IPR, Intel argued that a combination of figures from two references rendered obvious the segment-to-segment limitation. PACT did not necessarily dispute that the secondary reference showed this limitation but rather argued that Intel had failed to demonstrate a motivation to combine the references. Nonetheless, the PTAB found that the prior art did not teach the claimed segment-to-segment limitation. The PTAB further found that Intel had failed to show that a skilled artisan would have been motivated to combine the two references in the manner claimed. Intel appealed.

Issue/Holding:

Did the PTAB err in finding that the prior art failed to teach the segment-to-segment limitation and that Intel failed to show a motivation to combine the prior art? Yes, reversed.

Discussion:

On appeal, the Federal Circuit held that the secondary reference plainly illustrates the segment-to-segment limitation, noting that this was both Intel's and PACT's understanding at the PTAB proceedings.

Next, the Federal Circuit held that the PTAB's rejection of Intel's "known-technique" rationale was flawed. During the IPR, Intel had asserted that, because employing a separate cache was a known technique, it would have been obvious to use this teaching from the secondary reference to modify the primary reference. The PTAB disagreed, finding that the primary reference already addressed the same problem in a different manner (i.e., without the segmented cache), and thus a skilled artisan would not have needed to seek out the teachings of the secondary reference.

The Federal Circuit found the PTAB's conclusion improper, noting that the motivation-to-combine analysis is flexible and that the art does not need to provide precise teachings directed to the specific subject matter of the claim. Because both references are in the same field of endeavor and seek to address the same cache-coherency issue and because there was no dispute that the teachings of the secondary reference were used to improve cache coherency in multiprocessor systems, the Federal Circuit held that a skilled artisan would have been motivated to combine the references to improve cache coherency.

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