United States Court of Appeals for the Federal Circuit

ALACRITECH, INC.,
Appellant

v.

INTEL CORPORATION, CAVIUM, LLC, DELL, INC.,
Appellees

UNITED STATES,
Intervenor

2019-1467, 2019-1468

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2017-01409, IPR2017-01410, IPR2017-01736, IPR2017-01737, IPR2018-00338, IPR2018-00339.

Decided: July 31, 2020

SANFORD IAN WEISBURST, Quinn Emanuel Urquhart & Sullivan, LLP, New York, NY, for appellant. Also represented by JOSEPH M. PAUNOVICH, Los Angeles, CA.

GARLAND STEPHENS, Weil, Gotshal & Manges LLP, Houston, TX, for appellee Intel Corporation. Also represented by MELISSA LARUE HOTZE; GREGORY SILBERT, New York, NY; AMANDA BRANCH, ANNE MARIE CAPPELLA,

Redwood Shores, CA.

KARINEH KHACHATOURIAN, Rimon, P.C., Palo Alto, CA, for appellee Cavium, LLC. Also represented by NIKOLAUS A. WOLOSZCZUK.

KIRK T. BRADLEY, Alston & Bird LLP, Charlotte, NC, for appellee Dell, Inc. Also represented by EMILY CHAMBERS WELCH, Atlanta, GA; BRADY COX, Dallas, TX.

MELISSA N. PATTERSON, Appellate Staff, Civil Division, United States Department of Justice, Washington, DC, for intervenor. Also represented by ETHAN P. DAVIS, COURTNEY DIXON, SCOTT R. MCINTOSH; THOMAS W. KRAUSE, FARHEENA YASMEEN RASHEED, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA.

Before MOORE, CHEN, and STOLL, *Circuit Judges*.

STOLL, *Circuit Judge*.

Alacritech, Inc. appeals the Patent Trial and Appeal Board's final written decisions holding certain claims of U.S. Patent No. 8,131,880 unpatentable as obvious. We affirm in part, vacate in part, and remand. In particular, we hold that the Board did not adequately support its finding that the asserted prior art combination teaches or suggests a limitation recited in claims 41–43 of the '880 patent. We therefore vacate the Board's obviousness determination as to claims 41–43 and remand for further proceedings regarding those claims. We find no reversible error in the Board's remaining obviousness determinations. Accordingly, we affirm the Board's decisions in all other respects.

BACKGROUND

The '880 patent relates to computer networking, and is specifically directed to offloading certain network-related processing tasks from a host computer's central processing unit (CPU) to an "intelligent network interface card" (INIC). '880 patent Abstract. By offloading network processing tasks from the general-purpose CPU to the specialized hardware of the INIC, the invention purportedly improves performance by accelerating network communications while freeing the CPU to focus on other tasks. *See id.*

According to the '880 patent, one of the tasks that can be offloaded from the CPU to the INIC is the reassembly of data from packets received by the host computer from the network. *See id.* at col. 5 ll. 48–58, col. 76 ll. 17–22. Claim 41 is illustrative and recites "a flow re-assembler, disposed in the network interface" as follows:

> 41. An apparatus for transferring a packet to a host computer system, comprising:
>
> a traffic classifier, disposed in a network interface for the host computer system, configured to classify a first packet received from a network by a communication flow that includes said first packet;
>
> a packet memory, disposed in the network interface, configured to store said first packet;
>
> a packet batching module, disposed in the network interface, configured to determine whether another packet in said packet memory belongs to said communication flow;
>
> *a flow re-assembler, disposed in the network interface, configured to re-assemble a data portion of said first packet with a data portion of a second packet in said communication flow*; and

> a processor, disposed in the network interface, that maintains a TCP connection for the communication flow, the TCP connection stored as a control block on the network interface.

Id. at col. 93 l. 60 – col. 94 l. 12 (emphasis added to disputed claim limitation). Independent claim 43 similarly recites a "network interface comprising . . . a re-assembler for storing data portions of said multiple packets without header portions in a first portion of said memory." *Id.* at col. 94 ll. 32–41.

Appellees Intel Corporation, Cavium, LLC, and Dell Inc. (collectively, "Intel") petitioned for inter partes review of certain claims of the '880 patent. As relevant on appeal, Intel asserted that the challenged claims would have been obvious over Thia[1] in view of Tanenbaum.[2] In a pair of final written decisions, the Board agreed, holding all of the challenged claims unpatentable as obvious. *See generally Intel Corp. v. Alacritech, Inc.* (*'409 Decision*), No. IPR2017-01409, 2018 WL 5992621 (P.T.A.B. Nov. 14, 2018) (holding unpatentable claims 1, 5–10, 12, 14, 16, 17, 20–23, 27, 28, 45, and 55); *Intel Corp. v. Alacritech, Inc.* (*'410 Decision*), No. IPR2017-01410, 2018 WL 5992623 (P.T.A.B. Nov. 14, 2018) (holding unpatentable claims 32, 34, 35, 37–39, and 41–43).

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[1] Y.H. Thia & C.M. Woodside, *A Reduced Operation Protocol Engine (ROPE) for a Multiple-Layer Bypass Architecture*, *in* PROTOCOLS FOR HIGH SPEED NETWORKS IV 224 (G. Neufeld & M. Ito eds., 1995).

[2] ANDREW S. TANENBAUM, COMPUTER NETWORKS (3d ed. 1996).

Alacritech appeals the Board's obviousness determinations as to independent claims 1, 32, 41, and 43.[3] We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

I

On appeal, Alacritech argues that the Board's analysis is inadequate to support its finding that the asserted prior art teaches or suggests the reassembly limitations in claims 41–43. For the reasons that follow, we agree with Alacritech.

We review the Board's decisions under the standard set forth in the Administrative Procedure Act, which, in relevant part, requires us to set aside conclusions or findings that are "arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law," or "unsupported by substantial evidence." 5 U.S.C. § 706(2)(A), (E). To support our review, "the Board is obligated to 'provide an administrative record showing the evidence on which the findings are based, accompanied by the agency's reasoning in reaching its conclusions.'" *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019) (quoting *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002)). We do not require "perfect explanations," and "we will uphold a decision of less than ideal clarity if the agency's path may reasonably be discerned." *In re NuVasive, Inc.*, 842 F.3d 1376, 1382–83 (Fed. Cir. 2016) (quoting *Bowman Transp., Inc. v. Ark.-Best Freight Sys., Inc.*, 419 U.S. 281, 286 (1974)). We do, however,

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[3] Alacritech's appeal briefing also included a challenge to the appointment of the Administrative Patent Judges on the Board under the Appointments Clause of the Constitution, but this challenge has since been withdrawn and waived. *See* Dkt. No. 73.

require that the Board's own explanation be sufficient "for us to see that the agency has done its job." *Id.* at 1383.

The Board's analysis of the disclosure of the reassembly limitations in claims 41–43 falls short of that which the APA and our precedent require. After briefly reciting some of the parties' arguments in two terse paragraphs, the Board merely concludes that "data portions of packets are reassembled" in both claim 41 and the asserted prior art. *'410 Decision*, 2018 WL 5992623, at *5.[4] In doing so, the Board appears to misapprehend both the scope of the claims and the parties' arguments.

The claim limitations at issue require that reassembly take place in the network interface, as opposed to a central processor. *E.g.*, '880 patent col. 94 ll. 5–8 (claim 41 reciting "a flow re-assembler, *disposed in the network interface*, configured to re-assemble a data portion of said first packet with a data portion of a second packet in said communication flow" (emphasis added)); *see also id.* at col. 3 ll. 45–47 ("The present invention offloads network processing tasks from a CPU to a cost-effective intelligent network interface card (INIC)."). No party disputed that reassembly is disclosed by the asserted prior art. The crux of the dispute was *where* reassembly takes place in the prior art and whether that location satisfies the claim limitations. *See, e.g.*, J.A. 10247 (Intel arguing that "Thia . . . discloses a flow re-assembler *on the network interface* to re-assemble data portions of packets within a communication flow" (emphasis added)); J.A. 10577 (Alacritech responding that "[n]either Thia nor Tanenbaum discloses a flow re-assembler *that is part of the*

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[4] The Board did not separately address the similar reassembly limitation in independent claim 43, and the parties do not appear to have raised materially distinct arguments for that limitation. Thus, for the purposes of this appeal, claims 41–43 rise and fall together.

NIC" (emphasis added)). The Board's analysis does not acknowledge that aspect of the parties' dispute, much less explain how the prior art teaches or suggests reassembly in the network interface. As such, we cannot reasonably discern whether the Board followed a proper path in determining that the asserted prior art teaches or suggests the reassembly limitations, and by extension, that the subject matter of claims 41–43 would have been obvious.

Intel asserts that the Board adopted Intel's extensive discussion of the reassembly limitations in the petition by "favorably" citing to the petition in the final written decision. Appellees' Br. 25–26. We do not find this argument persuasive. Although the Board cited to the relevant portions of Intel's petition as it recounted certain arguments made by Intel, the Board did not endorse, adopt, or otherwise suggest that it was persuaded by those arguments, much less explain why it found those arguments persuasive. *See '410 Decision*, 2018 WL 5992623, at *5 (citing J.A. 10227–28, 10247–48); *see also Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993 (Fed. Cir. 2017) (rejecting Board's analysis as "inadequate" where it did not "cite, let alone explain or analyze or adopt" the relevant portion of the petition).

Intel also argues that it should prevail because the Board "soundly rejected" Alacritech's interpretation of Thia. Appellees' Br. 27. But the Board's rejection of certain arguments made by Alacritech does not necessarily support the Board's finding that the asserted prior art teaches or suggests reassembly in the network interface. *See NuVasive*, 842 F.3d at 1383 ("[I]t is not adequate to summarize and reject arguments without explaining why the [Board] accepts the prevailing argument."). That is especially the case here, where the parties' briefing focuses on the disclosure of the reassembly limitations by one reference (Thia), but the Board appears to have relied on a different reference (Tanenbaum) to support its finding.

Intel specifically argued in the petition that "[l]ike Tanenbaum[], Thia also discloses block data transfers to host memory, but *Thia adds that the transfer is from the network interface*." J.A. 10247 (emphasis added).[5] Intel maintained the same position on reply, contending that Alacritech's "argument regarding the flow re-assembler is based on an erroneous interpretation of *Thia*," and reiterating that Thia discloses a re-assembler in its network interface adaptor. J.A. 10736–37 (emphasis added). The Board nonetheless concluded that Alacritech had failed to establish "how the re-assembly of data portions of packets of *Tanenbaum (relied upon by Petitioner)* differs from the reassembly of data portions of packets, as recited in claim 41." *'410 Decision*, 2018 WL 5992623, at *5 (emphasis added). Because the Board's reasoning appears to be untethered to either party's position, we cannot infer

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[5] In the petition, Intel briefly argues in conclusory fashion that Tanenbaum "suggests that the re-assembler is provided on a network interface," but then immediately pivots to Thia, which assertedly "provides an express disclosure." J.A. 10247. The Board quoted this sentence without endorsement when it recounted Intel's arguments. *'410 Decision*, 2018 WL 5992623, at *5 (quoting J.A. 10247). As explained above, we do not interpret the Board's decision as having endorsed or adopted Intel's reassembly arguments. But even if the Board had endorsed or adopted Intel's conclusory statement regarding Tanenbaum, that would have been inadequate to support the Board's obviousness determination as to claims 41–43. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (alteration in original) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006))).

from the Board's rejection of one of Alacritech's arguments regarding Tanenbaum that the Board necessarily adopted Intel's position regarding Thia. That distinguishes this case from *Paice LLC v. Ford Motor Co.*, where "the Board's obviousness determinations flow[ed] directly from its rejection of [the patent owner's] arguments, and the Board's analysis [was] commensurate with [the patent owner's] arguments." 881 F.3d 894, 905 (Fed. Cir. 2018) (citing *Novartis AG v. Torrent Pharm. Ltd.*, 853 F.3d 1316, 1327–28 (Fed. Cir. 2017)).

After conceding that "the Board did not discuss in detail Alacritech's arguments regarding Thia," Intel insists that the substantial evidence standard requires us to affirm "so long as there is evidentiary support in the record, even if the support was not specifically cited by the Board." Appellees' Br. 28–29. This is a fundamentally incorrect statement of the law. In support, Intel musters only a footnote from a 2002 opinion of this court that, in response to a dissent, suggests without direct support that we may review the Board's factual findings just as we review those of a district court because we affirm judgments, not opinions. *See id.* at 29 (citing *In re Huston*, 308 F.3d 1267, 1281 n.9 (Fed. Cir. 2002)). But our precedent is clear: under the APA, "[o]ur review of a patentability determination is confined to 'the grounds upon which the Board actually relied.'" *TQ Delta*, 942 F.3d at 1358 (quoting *Power Integrations, Inc. v. Lee*, 797 F.3d 1318, 1326 (Fed. Cir. 2015)). And although our review under the APA is deferential, that "does not relieve the agency of its obligation to develop an evidentiary basis for its findings." *Id.* (quoting *Lee*, 277 F.3d at 1344). Indeed, the more recent precedents of *NuVasive* and its progeny—which include far more developed discussions of the APA than the footnote on which Intel relies—plainly establish that the Board is obligated to "articulate a satisfactory explanation for its action including a rational connection between the facts found and the choice made."

NuVasive, 842 F.3d at 1382 (quoting *Motor Vehicle Mfrs. Ass'n v. State Farm Mut. Auto. Ins. Co.*, 463 U.S. 29, 43 (1983)). Accordingly, we vacate the Board's obviousness determination as to claims 41–43 and remand for the Board to reconsider whether the asserted prior art teaches or suggests the entirety of the reassembly limitations, including the requirement that reassembly takes place in the network interface.

II

Alacritech raises two additional challenges on appeal, but we do not find them persuasive.

First, again addressing claims 41–43, Alacritech contests the Board's finding that an ordinarily skilled artisan would have been motivated to combine Thia and Tanenbaum. Specifically, Alacritech avers that Tanenbaum teaches away from the combination with Thia, and in any event the Board's conclusion otherwise is insufficient to support a motivation to combine.

We hold that the Board's finding of a motivation to combine Thia and Tanenbaum is supported by substantial evidence. A reasonable factfinder could conclude, as the Board did, that Tanenbaum merely expresses a preference and does not teach away from offloading processing from the CPU to a separate processor. *See, e.g.*, J.A. 2863 (Tanenbaum explaining that "*[u]sually*, the *best* approach is to make the protocols simple and have the main CPU do the work" (emphases added)); *see also Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017) ("A reference that 'merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into' the claimed invention does not teach away." (quoting *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013))). The Board's finding that an ordinarily skilled artisan would have been motivated to combine Thia and Tanenbaum is further supported by the Board's express en-

dorsement of other arguments offered by Intel in favor of the combination. *See '410 Decision*, 2018 WL 5992623, at *5–6. Alacritech does not specifically challenge this additional support for the Board's finding. Accordingly, we affirm the Board's finding of a motivation to combine. When the Board addresses claims 41–43 on remand, it need not reconsider its finding of a motivation to combine Thia and Tanenbaum.

Second, Alacritech challenges the Board's finding that the asserted prior art discloses the "operation code" limitation in claims 1 and 32. Each claim recites "associating an operation code" with a packet identified earlier in the claim, wherein the operation code indicates a status of that packet.[6] *E.g.*, '880 patent col. 90 ll. 1–6. Alacritech essentially seeks a narrowing interpretation that would limit the recited association to a direct mapping between one packet and one operation code. *See, e.g.*, Appellant's Br. 41 (arguing that "claims 1 and 32 expressly require that the operation code be associated with a particular packet (not a group of packets) and that it identify the status of said packet (not a group of packets)" (citing '880 patent col. 89 l. 59 – col. 90 l. 11 (claim 1), col. 93 ll. 3–28 (claim 32))). Alacritech provides no support for its interpretation beyond the language of the claims themselves.

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[6] Claim 1 recites "associating an operation code with said first packet, wherein said operation code indicates a status of said first packet, including whether said packet is a candidate for transfer to the host computer system that avoids processing said header portion by the host computer system in accordance with said TCP protocol." '880 patent col. 90 ll. 1–6. Claim 32 recites "associating an operation code with said packet, wherein said operation code identifies a status of said packet." *Id.* at col. 93 ll. 20–21.

We agree with the Board that the plain claim language, on its own, does not preclude an operation code from being associated with more than one packet. *See '409 Decision*, 2018 WL 5992621, at *3; *'410 Decision*, 2018 WL 5992623, at *4. That is especially so here, where the broadest reasonable interpretation applies.[7] Under the Board's correct interpretation, a reasonable factfinder could further find, as the Board did, that Thia teaches or suggests the recited operation code at least through its global flag, which is associated with the processing status of multiple received packets. *See '409 Decision*, 2018 WL 5992621, at *3; *'410 Decision*, 2018 WL 5992623, at *4. Thus, the Board's finding that the asserted prior art discloses the "operation code" limitation is supported by substantial evidence. We accordingly affirm the Board's obviousness determinations as to claims 1 and 32.

CONCLUSION

For the foregoing reasons, we vacate the Board's obviousness determination as to claims 41–43 and remand for further proceedings consistent with this opinion. We affirm the Board's decisions in all other respects.

AFFIRMED-IN-PART, VACATED-IN-PART, AND REMANDED

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[7] Per recent regulation, the Board applies the *Phillips* claim construction standard to IPR petitions filed on or after November 13, 2018. *See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (codified at 37 C.F.R. § 42.100(b)). Because Intel filed the petitions before November 13, 2018, the broadest reasonable interpretation standard applies to the IPR decisions on appeal.

COSTS

No costs.