IN RE RAMBUS, INC., Appeal No. 2013-1192 (Fed. Cir. June 4, 2014). Before Rader, Moore and Reyna. Appealed from Patent Trial and Appeal Board (PTAB).

Background:

Micron Technology Inc. initiated an *inter partes* reexamination of Rambus's patent. Micron argued that prior art U.S. Patent No. 4,734,909 (Bennett) disclosed "a register which stores *a value that is representative of an amount of time* to transpire after which the memory device outputs the first amount of data," (emphasis added) as recited in claim 26 of Rambus's patent. Bennett discloses a bus arbitration system including a plurality of bus lines and a clock, which is capable of operating based on eight configuration parameters I-VIII. Figs. 25a and 25b are timing charts based on the configuration parameter VI, in which the activities of signaling wait or transferring data are either multiplexed on the same line or have dedicated lines.

Micron argued that the multiplexed signals in Bennett's Fig. 25a cause a delay of known value (i.e., one clock cycle) before data transfer. Accordingly, setting parameter VI to 1 causes the signals to be multiplexed on the same line and create a one clock cycle delay before data transfer. The Board agreed with Micron that parameter VI corresponds to the claimed value, and thus found that Rambus's claims were anticipated by Bennett. Rambus appealed.

Issue/Holding:

Did the Board err in finding that Bennett anticipated Rambus's claims? Yes, reversed.

Discussion:

Rambus argued that Figs. 25a and 25b are simplified and hypothetical illustrations of how Bennett's invention works in theory and not actual schematics of Bennett's bus arbitration system. Rambus argued that, in practice, arbitration takes an unknown amount of time because a device may lose arbitration a number of times in a row. Rambus also argued that the wait signal may also delay the data transfer for an indeterminate amount of time if it indicates that the memory device is busy. Thus, Rambus argued that when Bennett's invention actually functions, it does not include a known delay time. Instead, Bennett's invention has an indefinite delay time based upon arbitration, busy memory devices, and other functions.

The Federal Circuit found that in Bennett's Figs. 25a and 25b, parameter VI is only "representative" of one source of delay because the actual delay can be longer due to other factors. For example, switching parameter VI from 3 to 1 does not necessarily create a one clock cycle delay before data is transferred due to further potential delay that may result from arbitration.

The Federal Circuit held that a value cannot "represent" an "amount of time" if there are additional factors, wholly unrepresented by that value, that necessarily impact, or represent, the "amount of time." Parameter VI is one factor that may affect the amount of time that passes before data is transferred but it does not represent that time. Accordingly, the Federal Circuit concluded that Bennett fails to disclose "a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data," and thus reversed the Board's decision that Bennett anticipates Rambus's patent.

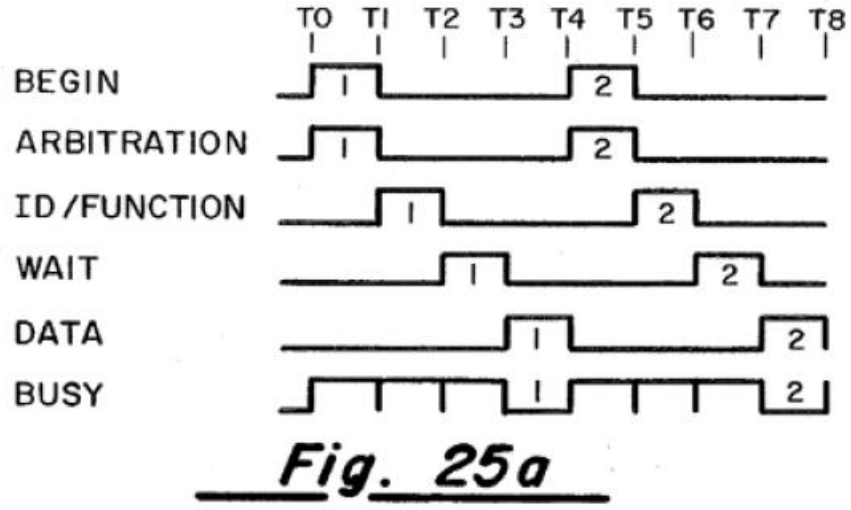


Fig. 25a

**Parameter VI = 1**
The data signal and the wait signal are multiplexed on the same line. Thus, the data transfer occurs one clock cycle later than the data transfer shown in Fig. 25b.

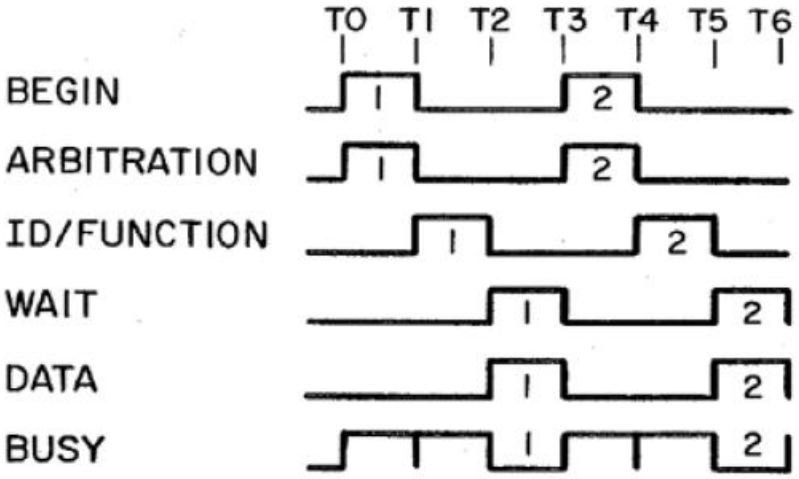


Fig. 25b

**Parameter VI = 3**
The data signal and the wait signal each have dedicated lines. Thus, the data transfer can occur at the same time as the transfer of the wait signal.